PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellant:	Bruce et al.	Examiner:	Hesseltine, R.
Application No.:	09/833,247	Group Art Unit:	2623
Filed:	April 11, 2001	Docket No.:	AMDA.486PA (TT4000)
Title:	Three-Dimensional Tomography		

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence and the papers, as described hereinabove, are being deposited in the United States Postal Service, as first class mail, in an envelope addressed to: Board of Patent Appeals and Interferences, United States Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450, on June 20, 2005.

By: Jennifer L. Larson

APPEAL BRIEF

Board of Patent Appeals and Interferences
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

Customer No.
40581

Sir:

This is an Appeal Brief submitted pursuant to 37 C.F.R. § 41.37 for the above-referenced patent application. Please charge Deposit Account No. 01-0365 (TT4000) in the amount of $500.00 for this brief in support of appeal as indicated in 37 C.F.R. § 41.20(b)(2). If necessary, authority is given to charge/credit deposit account 01-0365 (TT4000) any additional fees/overages in support of this filing.

I. Real Party in Interest

The real party in interest is the assignee, Advanced Micro Devices, Inc.

II. Related Appeals and Interferences

While Appellant is aware of other pending applications owned by the above-identified assignee, Appellant is unaware of any related appeals, interferences or judicial proceedings that would have a bearing on the Board's decision in the instant appeal.

III. Status of Claims

Claims 1-20 are presented for appeal because each of the appealed claims, 1-20, has been rejected. The pending claims under appeal, as presently amended, may be found in the attached Appendix of Appealed Claims.

IV. Status of Amendments

No amendments were filed subsequent to the final Office Action dated January 18, 2005.

V. Summary of Invention

In accordance with independent claim 1, one example embodiment of the present invention is directed to a method for analyzing a suspected defect in an integrated circuit die. *See, e.g.*, figures 1-4 and page 4, line 22 – page 7 line 19. The method includes removing substrate from a selected portion of the die to expose the suspected defect (*e.g.*, 120) (*see, e.g.*, figure 2 and page 6, lines 20-21) and recording a plurality of images of the selected portion as substrate is being removed therefrom (*see, e.g.*, page 6, lines 21-page 7, line 3). The method also includes creating a three-dimensional image of the selected portion of the die with the plurality of images and analyzing the die therefrom. *See, e.g.*, page 7, lines 7-19).

Another example embodiment of the present invention is directed to a system for analyzing a suspected defect in an integrated circuit die. *See, e.g.*, figure 7 and page 8, line 5 – page 9, line 4. The system includes means for removing substrate (*e.g.*, dual FIB/e-beam tomography device, FIB device, FEI XL830) from a selected portion of the die to expose the

suspected defect and means for recording a plurality of images of the selected portion (*e.g.*, dual FIB/e-beam tomography device, e-beam tomography device, FEI XL830) while substrate is being removed therefrom. The system also includes means for creating a three-dimensional image of the selected portion of the die with the plurality of images (*e.g.*, dual FIB/e-beam tomography device, FEI XL830, controller 740).

Another example embodiment of the present invention is directed to a system for analyzing a suspected defect in an integrated circuit die. *See, e.g.*, figure 7 and page 8, line 5 – page 9, line 4. The system includes a substrate removal arrangement (*e.g.*, 730) adapted to remove substrate from a selected portion of the die (*e.g.*, 720) to expose the suspected defect and an image recording arrangement (*e.g.*, 740/730) adapted to record a plurality of images of the selected portion while substrate is being removed therefrom. The system also includes an image creation arrangement (*e.g.*, 740/730) adapted to create a three-dimensional image of the selected portion of the die with the plurality of images recorded by the imaging arrangement.

As required by 37 C.F.R. § 41.37(c)(1)(v), a concise explanation of the subject matter defined in the independent claims involved in the appeal is provided herein. Appellant notes that representative subject matter is identified for these claims; however, the abundance of supporting subject matter in the application prohibits identifying all textual and diagrammatic references to each claimed recitation. Appellant thus submits that other application subject matter, which supports the claims but is not specifically identified above, may be found elsewhere in the application. Appellant further notes that this summary does not provide an exhaustive or exclusive view of the present subject matter, and Appellant refers to the appended claims and their legal equivalents for a complete statement of the invention.

VI. Grounds of Rejection

Claims 1-20 are rejected under 35 U.S.C. § 103(a) over Zimmerman *et al.* (U.S. Patent No. 6,162,735) in view of Phaneuf *et al.* (U.S. Patent No. 6,288,393).

VII. Argument

Appellant traverses the rejection of claims 1-20 because the Examiner has failed to satisfy each of the three requirements of a *prima facie* Section 103(a) rejection. In order to present a proper Section 103(a) rejection, the Examiner must present evidence of suggestion or motivation to combine the cited references, present a combination of references that teaches or suggests each of the claimed limitations, and have a reasonable expectation of success for the proposed combination. MPEP § 2143. Throughout the prosecution of this application, Appellant has shown that the Examiner has failed to satisfy any of these three criteria; therefore, the Section 103(a) rejection is improper and should be reversed.

Before addressing the specifics, Appellant notes that the Examiner's rejection is based on an *in-situ* defect analysis method as taught by the '735 reference in combination with an automated imaging method taught by the '393 reference for the purpose of reverse engineering. More particularly, the Examiner's rejection is based on the notion that a skilled artisan would be led to modify the *in-situ* defect analysis method of the '735 reference by the '393 reference's automated imaging as used for reverse engineering. Generally, Appellant submits that the Examiner proposes a combination of teachings that fails to be supported by evidence that a skilled artisan would be led to such a modification, that the proposed combination would not correspond to the claimed invention, and that the proposed combination would undermine the purpose of the primary '735 reference.

A. The rejection of claims 1-20 is improper because the Examiner fails to present evidence of motivation for the skilled artisan to combine the cited references, as asserted.

The Examiner's rejection is a combination of teachings, reconstructed by impermissible hindsight rather than properly based on evidence that a skilled artisan would be led to the asserted hypothetical embodiment. At page 3 of the final Office Action, the Examiner asserts that the motivation for the combination of teachings would be one of two possibilities. The first

possibility would be "to determine a schematic or other representation (such as a failure site or defect) of the circuitry (column 5, line 42-48)" according to some prior art implementation partially characterized by the '393 reference. This alleged motivation is illogical because the '735 *in-situ* method is a method for analyzing a failed chip to identify the defect. In order to analyze a failed chip to identify the defect, the analysis presupposes knowledge of the chip's operation and construction. For example, the '735 reference explains that the target location is typically a location believed to be the cause of the failure ('735 reference at column 1, lines 19-20), and this target location is then used as the target location for the *in-situ* etching taught by the '735 reference. To perform such an analysis, the analysis presupposes that the scientist performing the analysis is already in possession of the schematic that defines the chip's operation and construction. It is therefore illogical that a skilled artisan would implement any modification of the *in-situ* etching of the '735 reference in order "to determine a schematic" which the skilled artisan already possesses.

As part of this same first possibility, the Examiner also mentions as motivation, determining another "representation (such as a failure site or defect) of the circuitry." This assertion is also illogical because the '735 reference already teaches that the skilled artisan knows how to identify a failure site or defect of the circuitry per the express teachings of the '735 reference. No evidence or logic has been presented to support this first possibility.

The Examiner's second possibility is that the skilled artisan would have been led to implement the modification of the '735 reference for the purpose of "reverse engineering and integrated circuit analysis (column 9, line 44-49 [of the '393 reference]). As discussed above, this assertion must fail because the analysis of the '735 reference presupposes knowledge of the chip's schematic (which defines the chip's operation and construction).

Accordingly, the Examiner proposes modifying the '735 *in-situ* defect analysis method in a manner that teaches away from the '735 teachings. The '735 reference teaches an *in-situ* post-manufacture analysis of a semiconductor chip for which a schematic would have already been provided. In contrast, the teachings of the '393 reference are for a reverse engineering effort in order to determine the schematic for a particular circuit. The '393 reference is not directed to failure analysis but instead to automating reverse engineering of semiconductor chips in an *ex-situ* system that disregards the integrity of the chip once the process is complete. *See* the '393 reference at Abstract and Fig. 4. The '735 reference teaches directly away from the *ex-*

situ method employed by the '393 reference. Thus, the skilled artisan would not be led to combine the cited teachings as asserted and the rejection fails due to a lack of evidence of motivation. Appellant accordingly requests that the rejection be withdrawn.

B. The rejection of claims 1-20 is improper because the Examiner fails to identify where the cited references teach each of the claimed limitations.

The Examiner erroneously asserts that the '735 reference teaches recording a plurality of images of the selected portion as substrate is being removed therefrom at column 5, lines 15-46. However, the cited portion does not teach any recording of images. The '735 teachings merely disclose using a SEM to observe a target and make no mention of recording a plurality of images. A review of the '735 reference indicates no mention of the terms "image," "record," "save," and "picture." Without a presentation of correspondence to each of the claimed limitations, the Section 103(a) rejection is improper and cannot be maintained. Accordingly, Appellant requests that the rejection be reversed.

If the Examiner is asserting that the '735 observed images are inherently recorded or stored in some format, no evidence has been provided in support of such an assertion. In order to establish inherency, the extrinsic evidence "must make clear that the missing descriptive matter *is necessarily present in the thing described in the reference*, and that it would be so recognized by persons of ordinary skill." *Continental Can Co. v. Monsanto Co.*, 948 F.2d 1264, 1268, 20 U.S.P.Q.2d 1746, 1749 (Fed. Cir. 1991) (emphasis added). "Inherency, however, may not be established by probabilities or possibilities." *Id.* at 1269, 20 U.S.P.Q.2d at 1749 (quoting *In re Oelrich*, 666 F.2d 578, 581, 212 U.S.P.Q. 323, 326 (C.C.P.A. 1981). *See also*, MPEP § 2112. The Examiner fails to provide any of the requisite evidence in support of the apparent inherency assertion. No teachings have been identified in the '735 reference directed to recording images. In contrast to the Examiner's inherency conclusion, the '735 system appears to be directed to a system that merely allows observation of an etching process to provide visual confirmation as to the etch progression. *See, e.g.*, column 5, lines 40-46. Accordingly, the apparent inherency argument is unsupported and incorrect and therefore cannot be maintained.

With particular respect to the Official Notice taken at page 5, Appellant traversed this Notice and the Examiner did not appear to support the Official Notice as part of the finally-

rejected claims. Appellant fails to recognize, and no evidence has been presented in support of the assertion, that the skilled artisan would edit a three-dimensional image (as asserted) or that the skilled artisan would be able to obtain a corresponding three-dimensional image, as claimed. As discussed above, the '735 reference does not teach recording images with which to create a three-dimensional image. *See* MPEP § 2144.03. Thus, the skilled artisan would not be led to edit something that would not exist. Appellant accordingly requests that the rejection be reversed.

C. The rejection of claims 1-20 is improper because the Examiner's proposed combination would undermine the intended purpose of the reference being modified.

Without specifying how the teachings could be combined for operability, the Examiner proposes modifying the '735 *in-situ* defect analysis method to somehow include the *ex-situ* automated imaging method taught by the '393 reference for the purpose of reverse engineering a circuit. The '735 reference teaches *in-situ* throughout, and particularly in contrast to "[a]ll known methods for preparing and etching samples are *ex-situ* techniques." *See, e.g.,* the '735 reference column 1 in its entirety and especially at lines 39-40 and lines 65-66. The '393 etching method is an automated method that etches and subsequently images layers as the layers are removed, by employing steps that move the circuitry and equipment. The '393 reference uses a relatively complex *ex-situ* methodology involving multiple pieces of equipment, *e.g.,* as discussed in connection with figures 2 and 4, obtaining different images of the circuit to be reverse engineered. *See* column 6, lines 5 *et seq.*, and column 8, lines 18 *et seq*. Logically, the '393 reference does not mention or suggest any *in-situ* methodology or even consistent and/or a necessary use of a chamber in which its methodology could be implemented. These two methods are incompatible, and combining the specific teachings as asserted (to use the method of the '393 reference to obtain its 3-D image) would result in the '735 *in-situ* defect analysis method being transformed into a '735 *ex-situ* defect analysis method.

Appellant similarly disagrees with the Examiner's advisory comment (not part of the final Office Action) which argues that "the proposed combination only relies upon" the '393 reference's teaching needed to obtain 3-D imaging. Because the '393 reference teaches an

entire process (*e.g.*, figures 2 and 4) for obtaining such 3-D images and because the Examiner's advisory comment does not delineate any particular part of this entire process, Appellant respectfully submits that this comment is untenable and fails to provide any clarification. Moreover, because the '393 reference teaches an entire process for obtaining the 3-D images, the Examiner's advisory comment cannot escape the problems associated with the effort to combine the teachings.

More problematic is the fact that the '735 reference concerns a site-specific method for finding pinholes in dielectrics by observing an etch process in order to identify the pinholes, using an *in-situ* defect analysis. The '735 reference then explains how selective etching can be used to expand and highlight the pinholes for the defect analysis. In contrast to this pinhole-seeking method, the '393 reference teaches a process for etching off (removing) an entire layer of the '393 circuit. With the entire layer of the '393 circuit removed, the pinholes are removed as well. Thus, inclusion of the '393 automated etching/imaging method would replace the '735 method's observation aspects of the etch process and would undermine the purpose of the observation by removing the layers that would have defined any pinholes.

The MPEP states that when a proposed modification would render the teachings being modified unsatisfactory for their intended purpose or operation, then there is no suggestion or motivation to make the proposed modification under 35 U.S.C. § 103(a). *See* MPEP § 2143.01. A skilled artisan would not be led to modify the '735 teachings because the asserted modification would contradict the main objectives of providing an *in-situ* methodology and permitting the methodology to locate pinholes. Accordingly Appellant submits that the proposed combination is improper and requests that the rejection be withdrawn.

III. Conclusion

In view of the above, Appellant submits that the rejection is improper, the claimed invention is patentable, and that the rejection of claims 1-20 should be reversed. Appellant respectfully requests reversal of the rejection as applied to the appealed claims and allowance of the entire application.

Authority to charge the assignee's deposit account was provided on the first page of this brief.

Respectfully submitted,

CRAWFORD MAUNU PLLC
1270 Northland Drive – Suite 390
St. Paul, MN 55120
(651) 686-6633

By: _____
Name: Robert J. Crawford
Reg. No. 32,122

APPENDIX OF APPEALED CLAIMS

1. A method for analyzing a suspected defect in an integrated circuit die, the method comprising:

removing substrate from a selected portion of the die to expose the suspected defect;

recording a plurality of images of the selected portion as substrate is being removed therefrom; and

creating a three-dimensional image of the selected portion of the die with the plurality of images and analyzing the die therefrom.

2. The method of claim 1, wherein removing substrate includes cross-sectioning the die.

3. The method of claim 1, wherein removing substrate includes using a FIB.

4. The method of claim 1, wherein recording a plurality of images includes using a SEM.

5. The method of claim 1, wherein removing substrate includes using a FIB produced by a dual FIB/e-beam device, and wherein recording a plurality of images includes using the e-beam of the dual FIB/e-beam device to create a SEM image.

6. The method of claim 5, further comprising programming a controller adapted to control the dual FIB/e-beam device to effect the recording of a sufficient amount of SEM images to create a three-dimensional image of the selected portion.

7. The method of claim 1, wherein removing substrate from the selected portion includes exposing a defect in the die, and wherein creating a three-dimensional image includes creating a three-dimensional image of the defect.

8. The method of claim 1, wherein creating a three-dimensional image includes combining the plurality of images of the selected portion and creating a combined image therefrom.

9. The method of claim 1, further comprising using the three-dimensional image to detect a defect in the die.

10. The method of claim 9, wherein creating a three-dimensional image includes creating an image of the defect, further comprising using the image of the detected defect to analyze the defect.

11. The method of claim 1, wherein creating a three dimensional image includes using selected ones of the plurality of images of the selected portion to create a three dimensional image of less than the entire selected portion.

12. The method of claim 1, further comprising editing the three dimensional image to create an edited image of only a portion of the three-dimensional image.

13. The method of claim 12, wherein editing the three-dimensional image includes creating an image of a cross-section of the selected portion.

14. A system for analyzing a suspected defect in an integrated circuit die, the system comprising:

means for removing substrate from a selected portion of the die to expose the suspected defect;

means for recording a plurality of images of the selected portion while substrate is being removed therefrom; and

means for creating a three-dimensional image of the selected portion of the die with the plurality of images.

15. A system for analyzing a suspected defect in an integrated circuit die, the system comprising:

a substrate removal arrangement adapted to remove substrate from a selected portion of the die to expose the suspected defect;

an image recording arrangement adapted to record a plurality of images of the selected portion while substrate is being removed therefrom; and

an image creation arrangement adapted to create a three-dimensional image of the selected portion of the die with a plurality of images recorded by the imaging arrangement.

16. The system of claim 15, wherein the substrate removal arrangement includes a FIB device

17. The system of claim 15, wherein the image recording arrangement includes an e-beam device adapted to create a SEM image.

18. The system of claim 15, wherein the substrate removal arrangement and the image recording arrangement are included in a single dual FIB/e-beam device adapted to remove substrate with the FIB and to create a SEM image with the e-beam.

19. The system of claim 18, wherein the image creation arrangement is adapted to use the SEM image to create the three-dimensional image.

20. The system of claim 15, wherein the image creation arrangement includes a computer adapted to create the three-dimensional image in response to image characteristic selections.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.